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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301919-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kevin B. Leigh et al.

Confirmation No.: 2616

Application No.: 09/872,600

Examiner: Huynh, Kim T.

Filing Date: 06/01/2001

Group Art Unit: 2112

Title: System and Method of Automatically Switching Control of a Bus in a Processor-Based Device

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **3/24/2005**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
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( )	three months	$1020.00
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( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kevin B. Leigh et al.	§	Group Art Unit: 2112
Serial No.: 09/872,600	§	Examiner: HUYNH, KIM T
Filed: June 1, 2001	§	
For: SYSTEM AND METHOD OF AUTOMATICALLY SWITCHING CONTROL OF A BUS IN A PROCESSOR-BASED DEVICE	§	Atty. Docket: COMP:0213/FLE (200301919-1)

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May 24, 2005 — Date

David M. Hoffman

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Commissioner for Patents
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Alexandria, VA 22313

Sir:

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on March 24, 2005, and received by the Patent Office on March 28, 2005.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be necessary to advance prosecution of the present application, to Account No. 08-2025, Order No. 200301919-1/FLE (COMP:0213).

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1. **REAL PARTY IN INTEREST**

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas and the Assignee of the above-referenced application. The Assignee of the above-referenced application will be directly affected by the Board's decision in the pending appeal.

2. **RELATED APPEALS AND INTERFERENCES**

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. **STATUS OF CLAIMS**

Claims 1-55 are currently pending, are currently under final rejection and, thus, are the subject of this appeal.

4. **STATUS OF AMENDMENTS**

No claims have been amended since the final rejection. As such, there are no outstanding amendments to be considered by the Board.

5. **SUMMARY OF CLAIMED SUBJECT MATTER**

The present application is directed to a system and method of automatically switching control of a bus in a processor-based device. Page 2, lines 7-8. While certain system motherboards may include a controller for controlling devices on a bus, such as a SCSI controller for controlling SCSI devices, many end-users may desire incorporation of alternate controller cards which provide different or additional features. Page 3, line 21 - page. 4, line

2. Accordingly, in one exemplary embodiment, when a SCSI expansion card is connected to the expansion port, a presence detect signal is automatically asserted, thereby indicating the presence of the SCSI expansion card. Pg. 10, lines 8-11. When a SCSI expansion card is not connected to the expansion port, a switch couples the locally resident controller to the SCSI back plane, thereby enabling control of the SCSI devices by the locally resident SCSI controller. Pg. 12, lines 9-11. Conversely, when the SCSI expansion card is connected to the expansion port, the presence detect signal is asserted, which causes the switch to decouple the locally resident SCSI controller from the SCSI bus segment, thereby enabling control of the bus and the SCSI devices on the bus by a controller on the SCSI expansion card. Pg. 12, lines 15-21.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus (e.g., 50) in a processor-based device (e.g., 10). *See, e.g.,* page 8, lines 19-22; *see also* Fig. 3. The method comprises the act of electrically coupling a first bus controller (e.g., 42) to the bus. *See, e.g.,* page 7, lines 20-22. The method also includes generating a detection signal (e.g., 82) indicative of coupling of a second bus controller (e.g., 32) to the bus. *See, e.g.,* page 10 lines 5-17; *see also*, page 12, lines 15-22. The method also comprises automatically isolating the first bus controller from the bus in response to the detection signal. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 13, discussions of the recited features of claim 13 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus in a processor-based device (e.g. 10), the processor-based device comprising a first bus controller (e.g., 42) and a bus disposed on a first substrate (e.g., 28), wherein the first bus controller is coupled to the bus and configured to control the bus. *See, e.g.,* page 8, lines 15-22; *see also* Fig. 3. The method comprises the act of electrically coupling a second bus controller (e.g., 32) to the bus. *See, e.g.,* page 7, lines 20-22. The method also includes detecting presence of the second bus controller. *See, e.g.,* page 10, lines 1-3. The method further includes automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 21, discussions of the recited features of claim 21 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus in a low profile server (e.g., 10), the low profile server comprising a first bus controller (e.g., 42), a bus, and an isolation device (e.g., 72), wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate the first bus controller from the bus. *See, e.g.,* page 8, line 15 – page 9, line 7; *see also, e.g.,* page 12, lines 7-13; *see also* Fig. 3. The method comprises the act of connecting a second bus controller (e.g., 32) to the bus to cause the isolation device to isolate the first bus controller from the bus. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 23, discussions of the recited features of claim 23 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a processor-based device (e.g., 10). *See, e.g.,* page 8, line 15 – page 9, line 7; *see also* Fig. 3. The device comprises a processor (e.g., 36) and a memory (e.g., 40) coupled to the processor. *See, e.g.,* page 8, lines 1-13. The device also comprises a first substrate (e.g., 28). The first substrate includes a bus disposed on the first substrate. *See, e.g.,* page 8, lines 1-15. The first substrate also comprises a first bus controller (e.g., 42) disposed on the first substrate, the first bus controller being coupled to the processor and to the bus. *See, e.g.,* page 8, lines 1-15. The first substrate also includes an isolation device (e.g., 72) disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller (e.g., 32) coupled to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.*, page 12, line 15 – page 13, line 3.

With regard to the aspect of the invention set forth in independent claim 35, discussions of the recited features of claim 35 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a printed circuit board (e.g., 28) for a low profile server (e.g., 10). *See, e.g.,* page 7, lines 4-22. The board comprises a substrate (e.g., 28) and a bus disposed on the substrate. *See, e.g.,* page 8, lines 1-15. The board also includes a first bus controller (e.g., 42) disposed on the substrate, the first bus controller coupled to the bus and configured to control the bus. *See, e.g.,* page 8, lines 1-15; *see also e.g.*, page 12, line 15 –

page 13, line3. The board also includes an isolation device (e.g., 72) disposed on the substrate and configured to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.*, page 12, line 15 – page 13, line 3.

With regard to the aspect of the invention set forth in independent claim 44, discussions of the recited features of claim 44 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of manufacturing a device (e.g., 10) for switching control of a bus in a processor-based device. *See, e.g.,* page 8, lines 19-22; *see also* Fig. 3. The method comprises the act of providing a bus disposed on a substrate (e.g., 28). *See, e.g.,* page 7, lines 20-22. The method also includes connecting an expansion port (e.g., 55) to the bus, the expansion port being configured for connection to a second bus controller (e.g., 32). *See, e.g.,* page 12, lines 15-22. The method further comprises disposing an isolation device (e.g., 72) on the substrate, the isolation device being connected to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.,* page 12, lines 7-13. The method also comprises disposing a first bus controller (e.g., 42) on the substrate, the first bus controller being connected to the isolation device, the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 52, discussions of the recited features of claim 52 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of manufacturing an expansion card (e.g., 32)

connectable to a system controller board (e.g., 28) having a system bus controller (e.g., 42) configured to control the bus, and having an isolation device (e.g., 72). *See, e.g.,* page 8, lines 1-13 and 19-22; *see also, e.g.,* page 12, lines 7-13; *see also* Fig. 6. The method comprises the act of disposing an expansion bus controller (e.g., 42) on a substrate, the expansion bus controller being configured to control a bus. *See, e.g.,* page 8, line 19 – page 9, line 7. The method also comprises disposing a detect signal generator (e.g., 55) on the substrate. *See, e.g.,* page 12, lines 15-22; *see also* Fig. 6. The method also includes connecting the detect signal generator to the first expansion connector (e.g., 32); *see, e.g.,* page 12, lines 15-22. The method also comprises disposing a first expansion connector(e.g., 55) on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator, wherein the first expansion connector is configured to couple with a cable (e.g., 62), the cable having a first end (e.g., 70) connectable to the first expansion connector and a second end (e.g., 66) connectable to a system controller board (e.g., 28) and wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable and wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal. *See, e.g.,* page 9, lines 9-17, page 10, lines 1-3, and page 12, lines 7-22.

With regard to the aspect of the invention set forth in independent claim 53, discussions of the recited features of claim 53 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching between a first device (e.g., 42) and a second device (e.g., 32) connectable to a communications medium in a processor-based device (e.g., 10). *See, e.g.,* page 8, lines 1-13 and 19-22; *see also, e.g.,* page 12, lines 7-13; *see also*

Fig. 6. The method comprises the act of electrically coupling a first device to the communications medium. *See id.* The method also includes generating a detection signal indicative of coupling of a second device to the communications medium. *See, e.g.,* page 9, lines 9-17, page 10, lines 1-3, and page 12, lines 7-22. The method also comprises automatically isolating the first device from the communications medium in response to the detection signal. *See id.*

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1-10, 12-21, 23-31, 35-41, 43-50, and 52-55 under 35 U.S.C. § 102(b) as being anticipated by Vivio (U.S. Patent No. 5,706,447 hereafter "the Vivio reference").

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of Applicant's Admitted Prior Art (hereafter, "AAPA").

Third Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's third ground of rejection in which the Examiner rejected claims 32-34, 42, and 51 under 35

U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of Gasparik et al. (U.S. Patent No. 6,072,943, hereafter "the Gasparik reference").

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Sections 102 and 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-55 are currently in condition for allowance.

A. First Ground of Rejection

The Examiner rejected claims 1-10, 12-21, 23-31, 35-41, 43-50, and 52-55 under 35 U.S.C. § 102(b) as being anticipated by the Vivio reference. Appellants respectfully traverse these rejections. Each of the independent claims will be discussed separately below.

1. Judicial precedent has clearly established a legal standard for a prima facie anticipation rejection.

Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 227 U.S.P.Q. 773 (Fed. Cir. 1985). Thus, for a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). Moreover, the prior art reference also must show the *identical* invention "*in as complete detail as contained in the ... claim*" to support a *prima facie* case of anticipation. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989) (emphasis

added). Accordingly, Appellants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter.

2. **The Examiner's rejection of independent claim 1 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 1 recites:

> A method of switching control of a bus in a processor-based device, the method comprising the acts of:
> electrically coupling a first bus controller to the bus;
> generating a detection signal indicative of coupling of a second bus controller to the bus; and
> automatically isolating the first bus controller from the bus in response to the detection signal.

In rejecting independent claim 1, the Examiner asserted that the Vivio reference discloses all of the recited features of the claim. *See* Official Action mailed August 10, 2004, page 2. Appellants respectfully traverse this assertion.

As discussed above, the present application discloses a system and method of automatically switching control of a bus in a processor-based device. Page 2, lines 7-8. In one exemplary embodiment, to enable a user to install an alternative controller on an expansion card via an I/O port, a locally resident bus controller is coupled to a switch/terminator module to automatically switch control of the bus and the devices on the bus from the locally resident bus controller to a bus controller on an expansion card whenever an expansion card is connected to the expansion port. Page 8, line 20 - page 9, line 4. When an expansion card is connected to the system motherboard, the locally resident bus controller is isolated from the bus such that a controller on the expansion card can assume control of the bus and the devices on the bus. Page 10, lines 1-3.

Accordingly, independent claim 1 recites a method for automatically isolating a first bus controller from the bus in response to a detection signal that is indicative of coupling a second bus controller to the bus. In sharp contrast, the Vivio reference discloses neither switching control of a bus nor isolating a first bus controller from the bus. As explained to the Examiner in the Appellants' Response to Office Action mailed October 27, 2004, the Vivio reference merely discloses "a system for automatically maintaining proper bus termination." Abstract, lines 1-2. As stated in the Description of the Related Art section of the Vivio reference:

> it is desirable for the P6 processors to be located at the ends of the bus for signal quality reasons....However, this type of architecture creates difficulties for maintaining proper bus termination [because in the]...case where no module is plugged into a connector at one end of the bus, termination must be provided on the PCB motherboard [but in the]...case where a processor is plugged into the connector at one end of the bus, the effective end of the bus changes [from the PCB motherboard] to be located on the processor module. Thus to maintain proper termination, the termination on the motherboard must be removed, and the bus must be terminated at the effective bus end on the processor module. Col. 3, lines 6-24.

To address the problem set forth above, the Vivio reference discloses a system that permits the bus termination point to switch from the motherboard to the processor module. *See* col. 4, lines 27-36. Specifically, looking at Fig. 5 of the Vivio reference, when the processor module 542 is inserted into the connector 210, the terminator 224 is switched off by the switching device 222. This allows the terminator 548, which is located on the processor module 542, to become the termination point for that side of the bus. ***See*** col. 8, lines 50-66. If the processor module 542 is removed from the connector 210, the switching

device 222 is switched on, and the terminator 224 once again becomes the termination point for that side of the bus. *See* col. 8, line 63 – col. 9, line 4.

Appellants note that the section of the Vivio reference cited by the Examiner to anticipate claim 1 describes two separate structures (the processor modules 512 and 542) but the Examiner has not correlated these structures with the respectively recited "first bus controller," and "second bus controller," as recited in claim 1. *See* Office Action mailed August 10, 2004, page 2, lines 12-16. Both possibilities will be considered below and, regardless of which reading was intended by the Examiner, features of claim 1 are clearly missing from the Vivio reference.

First, the Vivio reference does not anticipate claim 1 if the processor module 512 is considered to be the first bus controller and the processor module 542 is considered to be the second bus controller. Hypothetically, if the processor module 512 is considered to be the recited first bus controller, the first step of claim 1 would entail coupling the processor module 512 to the bus 120. For the next step of claim 1, a detection signal would need to be generated when the processor module 542 (the hypothetical second bus controller) is coupled to the bus 120. When the processor module 542 is coupled to the connector 210, the termination point for the bus 120 would move from the terminator 224 to the terminator 548 located in the processor module 542. *See* Vivio, col. 8, lines 50-62; *see also*, Fig. 5. However, because the Vivio reference discloses a system that facilitates the use of *dual processors*, any detection signal generated after the processor module 542 is coupled to the bus 120 would not automatically isolate the processor module 512 from the bus 120. In fact,

the system disclosed in the Vivio reference *purposely does not isolate* the processor module 512 to facilitate the addition of a second processor to increase the computing power of the computer system 100. *See* Vivio, col. 4, lines 1-17. As such, the Vivio reference cannot anticipate claim 1 if the processor module 512 is considered to be the first bus controller and the processor module 542 is considered to be the second bus controller.

Similarly, the Vivio reference does not anticipate claim 1 if the processor module 542 is considered to be the first bus controller and the processor module 512 is considered to be the second bus controller. In this hypothetical reading of the Vivio reference, the processor module 542 would first be electrically coupled to the bus 120. When the processor module 542 is coupled to the connector 210, the termination point for the bus 120 would move from the terminator 224 to the terminator 548 located in the processor module 542. *See* Vivio, col. 8, lines 50-62; *see also*, Fig. 5. Next, a detection signal would be generated when the processor module 512 is coupled to the bus 120. However, similar to the first hypothetical scenario outlined above, the processor module 542 would not be automatically isolated from the bus 120 in response to this detection signal. In fact, the Vivio reference makes it clear that the only event that could cause the termination point to shift back from the terminator 548 to the terminator 224 is the physical removal of the processor module 542 by a user. *See id.* However, if the processor module 542 is physically removed from the connector 210, it is not being "automatically isolated...*in response to the detection signal*," as recited in claim 1. For this reason, it is clear that the Vivio reference does not anticipate independent claim 1 if the processor module 542 is considered to be the first bus controller and the processor module 512 is considered to be the second bus controller.

From the discussion above, it is clear that no matter how the elements in the Vivio reference are considered, the Vivio reference does not anticipate claim 1. While Appellants do not dispute that the Vivio reference discloses two bus controllers and two bus terminators, the Examiner has simply not provided any evidence that the apparatus of the Vivio reference discloses or suggests employing these elements in the manner recited in claim 1. Specifically, the Vivio reference does not disclose isolating the first bus controller from the bus, as recited in claim 1, much less automatically isolating the first bus controller from the bus in response to a detection signal, as further recited in claim 1. For at least this reason, Appellants respectfully assert that the Examiner has clearly not established a *prima facie* case of anticipation with regard to claim 1. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claim 1 and the claims that depend therefrom.

3. **The Examiner's rejection of independent claim 13 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 13 recites:

> A method of switching control of a bus in a processor-based device, the processor-based device comprising a first bus controller and a bus disposed on a first substrate, wherein the first bus controller is coupled to the bus and configured to control the bus, the method comprising the acts of:
> electrically coupling a second bus controller to the bus;
> detecting presence of the second bus controller; and
> automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller.

The Vivio reference fails to disclose every element of independent claim 13. For example the Vivio reference does not disclose "automatically *switching control* of the

bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller." (Emphasis added). First, it is important to note that the Examiner has not even suggested that the Vivio reference discloses "automatically switching control," as recited in claim 13. *See* Office Action mailed August 10, 2004, page 2, lines 10-16. Instead, the Examiner has rejected independent claim 13 based solely on the features of independent claim 1. *See id.* As claim 1 does not recite "automatically switching control of the bus," as recited in claim 13, the Examiner's rejection clearly cannot establish a *prima facie* case of anticipation.

Next, in the Office Action mailed August 10, 2004, the Examiner cites col. 4, lines 18-62 from the Vivio reference to support the rejection of independent claims 1 and 13. However, this section of the Vivio relates to switching the termination point of a SCSI bus – not to "switching control of the bus," as recited in claim 13. *See* Vivio, col. 4, lines 18-62. Moreover, there is virtually no discussion in the Vivio reference regarding control of the computer bus 120, much less "switching control of the bus," as recited in claim 13. In fact, the Vivio reference only uses the words "bus" and "control" in the same sentence once, and that use is clearly unrelated to bus control as it involves interrupt control devices. *See* col. 5, lines 62-67.

Moreover, the very idea of switching control from one bus to another is antithetical to the operating concept of the Vivio reference. Specifically, as described above, the Vivio reference is directed towards a system that facilitates the addition or removal of an additional processor to a computer system. *See* Vivio, col. 8, lines 50-62; *see also*, Fig. 5. This second processor is intended to work in conjunction with the first

processor and not to take control of the bus 120. *See id.* For this reason, it is clear that the Vivio reference does not disclose "automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller," as recited in claim 13.

Because the reference fails to disclose each element recited in claim 13, the Vivio reference fails to anticipate independent claim 13. Thus, the Examiner's rejection of independent claim 13, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 13 and its dependent claims.

4. **The Examiner's rejection of independent claim 21 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 21 recites:

> A method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate the first bus controller from the bus, the method comprising the act of:
> connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus.

The Vivio reference fails to disclose every element of independent claim 21. Appellants note that independent claim 21 recites "connecting a second bus controller to the bus *to cause the isolation device to isolate the first bus controller* from the bus." (Emphasis added). As summarized above with respect to the improper rejection of claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 21. Thus, the Examiner's rejection of independent claim 21, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 21 and the claims that depend from it.

5. **The Examiner's rejection of independent claim 23 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 23 recites:

> A processor-based device, comprising:
> a processor;
> a memory coupled to the processor; and
> a first substrate, comprising:
> a bus disposed on the first substrate;
> a first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and to the bus; and
> an isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

The Vivio reference fails to disclose every element of independent claim 23. Appellants note that independent claim 23 recites "an isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and *to automatically isolate the first bus controller from the bus* in response to detection of a second bus controller coupled to the bus." (Emphasis added). As summarized above with respect to the improper rejection of claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 23. Thus, the Examiner's rejection of independent claim 23, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 23 and the claims that depend from it.

6. **The Examiner's rejection of independent claim 35 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 35 recites:

> A printed circuit board for a low profile server, the system board comprising:
> a substrate;
> a bus disposed on the substrate;
> a first bus controller disposed on the substrate, the first bus controller coupled to the bus and configured to control the bus; and
> an isolation device disposed on the substrate and configured to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

The Vivio reference fails to disclose every element of independent claim 35. Appellants note that independent claim 35 recites "an isolation device disposed on the substrate and configured *to automatically isolate the first bus controller* from the bus in response to detection of a second bus controller coupled to the bus." (Emphasis added). As summarized above with respect to the improper rejection of claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 35. Thus, the Examiner's rejection of

independent claim 35, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 35 and the claims that depend from it.

7. **The Examiner's rejection of independent claim 44 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 44 recites:

> A method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:
> providing a bus disposed on a substrate;
> connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller;
> disposing an isolation device on the substrate, the isolation device being connected to the bus; and
> disposing a first bus controller on the substrate, the first bus controller being connected to the isolation device, the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port.

The Vivio reference fails to disclose every element of independent claim 44. Appellants note that independent claim 44 recites "disposing a first bus controller on the substrate, the first bus controller being connected to the isolation device, *the isolation device being configured to isolate the first bus controller from the bus.*" (Emphasis added). As summarized above with respect to the improper rejection of claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 44. Thus, the Examiner's rejection of

independent claim 44, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 44 and the claims that depend from it.

8. **The Examiner's rejection of independent claim 52 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 52 recites:

> A method of manufacturing an expansion card connectable to a system controller board having a system bus controller configured to control the bus, and having an isolation device, the method comprising the acts of:
>
> disposing an expansion bus controller on a substrate, the expansion bus controller being configured to control a bus;
>
> disposing a detect signal generator on the substrate;
>
> connecting the detect signal generator to the first expansion connector; and
>
> disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator,
>
> wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board,
>
> wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable, and
>
> wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal.

The Vivio reference fails to disclose every element of independent claim 52. Appellants note that independent claim 52 recites an isolation device "wherein the isolation device is configured *to isolate the system bus controller from the bus* in response to the detect signal." (Emphasis added). As summarized above with respect to the improper rejection of

claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 52. Thus, the Examiner's rejection of independent claim 52, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 52 and the claims that depend from it.

8. **The Examiner's rejection of independent claim 53 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 53 recites:

> A method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:
>
> electrically coupling a first device to the communications medium;
>
> generating a detection signal indicative of coupling of a second device to the communications medium; and
>
> automatically isolating the first device from the communications medium in response to the detection signal.

The Vivio reference fails to disclose every element of independent claim 53. Appellants note that independent claim 53 recites an isolation device "*automatically isolating the first device* from the communications medium in response to the detection signal." (Emphasis added). As summarized above with respect to the improper rejection of claim 1, the arguments for which are incorporated herein by reference, the Vivio reference does not disclose isolating the first bus controller.

Because the reference fails to disclose each element recited by the instant claim, the Vivio reference fails to anticipate independent claim 53. Thus, the Examiner's rejection of independent claim 53, and the claims depending therefrom, is clearly improper. Accordingly, Appellants request the Board overturn the rejection and allow independent claim 53 and the claims that depend from it.

B. **Second and Third Grounds of Rejection**

1. **Judicial precedent has clearly established a legal standard for a prima facie obviousness rejection.**

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes all of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

2. **The Examiner's rejection of independent claims 11, 22, and 34 is improper because the rejection fails to establish a prima facie case of obviousness.**

The Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447) in view of Applicant's Admitted Prior Art ("AAPA"). Appellants respectfully traverse these rejections.

Claims 11, 22, and 34 depend from independent claims 1, 21, and 23, respectively, each of which is discussed above. Moreover, each of the Examiner's obviousness rejections is based primarily on the Vivio reference, which is also discussed above. With this in mind, Appellants respectfully assert that the Applicant's Admitted Prior Art employed in conjunction with the Vivio reference, does not obviate the deficiencies of the Vivio reference as discussed in the foregoing remarks regarding the Examiner's rejections of independent claims 1, 21, and 23. Accordingly, Appellants respectfully assert that claims 11, 22, and 34 are not only patentable for their dependencies on an allowable base claims but also by virtue of the additional features recited therein.

In light of the forgoing remarks, Appellants respectfully request that the Board withdraw the obviousness rejections in relation to claims 11, 22, and 34. Additionally, Appellants respectfully request that the Board direct the Examiner to allow these claims.

3. **The Examiner's rejection of independent claims 32-34, 42, and 51 is improper because the rejection fails to establish a prima facie case of obviousness.**

The Examiner rejected claims 32-34, 42, and 51 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447) in view of Gasparik et al. (U.S. Patent No. 6,072,943). Appellants respectfully traverse these rejections.

Claims 32-34, 42, and 51 depend from independent claims 23, 35, and 44, respectively, each of which is discussed above. Moreover, each of the Examiner's obviousness rejections is based primarily on the Vivio reference, which is also discussed above. With this in mind, Appellants respectfully assert that the Gasparik reference employed in conjunction with the Vivio reference does not obviate the deficiencies of the Vivio reference as discussed in the foregoing remarks regarding the Examiner's rejections of independent claims 23, 35, and 44. Accordingly, Appellants respectfully assert that claims 32-34, 42, and 51 are not only patentable for their dependencies on allowable base claims but also by virtue of the additional features recited therein.

In light of the forgoing remarks, Appellants respectfully request that the Board withdraw the obviousness rejections in relation to claims 32-34, 42, and 51. Additionally, Appellants respectfully request that the Board direct the Examiner to allow these claims.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: May 24, 2005

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8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1. A method of switching control of a bus in a processor-based device, the method comprising the acts of:

electrically coupling a first bus controller to the bus;

generating a detection signal indicative of coupling of a second bus controller to the bus; and

automatically isolating the first bus controller from the bus in response to the detection signal.

2. The method as recited in claim 1, comprising the act of terminating the first bus controller.

3. The method as recited in claim 2, wherein the first bus controller is terminated in response to detection of the detection signal.

4. The method as recited in claim 1, wherein the bus comprises a plurality of traces disposed on a substrate, wherein the first bus controller is electrically coupled to a first segment of the plurality of traces, and wherein the second bus controller is electrically coupled to a second segment of the plurality of traces.

5. The method as recited in claim 4, comprising the act of terminating the second segment of the plurality of traces.

6. The method as recited in claim 5, comprising the act of electrically removing termination of the second segment of the plurality of traces in response to detection of the second bus controller.

7. The method as recited in claim 1, wherein the first bus controller is disposed on a first substrate, and the second controller is disposed on a second substrate, the second substrate being coupled to the first substrate, and wherein the act of generating a detection signal comprises the act of transmitting the detection signal from the second substrate to the first substrate.

8. The method as recited in claim 7, wherein the first substrate comprises an expansion port, and a first end of the cable is connected to the expansion port.

9. The method as recited in claim 1, wherein the bus comprises a SCSI bus.

10. The method as recited in claim 7, wherein the first substrate and the second substrate each comprise a printed circuit board.

11. The method as recited in claim 7, wherein the first substrate and the second substrate are disposed within a low profile server.

12. The method as recited in claim 1, wherein the act of electrically coupling comprises the act of coupling the first bus controller to the bus using a switch.

13. A method of switching control of a bus in a processor-based device, the processor-based device comprising a first bus controller and a bus disposed on a first substrate, wherein the first bus controller is coupled to the bus and configured to control the bus, the method comprising the acts of:

electrically coupling a second bus controller to the bus;

detecting presence of the second bus controller; and

automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller.

14. The method as recited in claim 13, wherein the act of detecting the presence of the second bus controller comprises the act of generating a detect signal when the second bus controller is electrically coupled to the bus.

15. The method as recited in claim 13, wherein the act of automatically switching control of the bus comprises the acts of:

isolating the first bus controller from the bus; and

terminating the isolated first bus controller.

16. The method as recited in claim 13, comprising the act of terminating the bus proximate the first bus controller.

17. The method as recited in claim 14, wherein the bus is terminated proximate the first bus controller in response to detecting the presence of the second bus controller.

18. The method as recited in claim 15, wherein the second bus controller is disposed on a second substrate coupled to the first substrate.

19. The method as recited in claim 18, wherein the first substrate comprises an expansion port, and the method comprises the act of terminating the bus proximate the expansion port.

20. The method as recited in claim 19, comprising the act of removing termination of the bus proximate the expansion port in response to detecting the presence of the second bus controller.

21. A method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate the first bus controller from the bus, the method comprising the act of:

connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus.

22. The method as recited in claim 21, wherein the first bus controller is disposed on a first substrate, and wherein the second bus controller is disposed on a second substrate, and the act of connecting the second bus controller to the bus comprises the acts of:

disposing a cable in the low profile server, the cable comprising a first end and a second end;

connecting the first end of the cable to the first substrate; and

connecting the second end of the cable to the second substrate.

23. A processor-based device, comprising:

a processor;

a memory coupled to the processor; and

a first substrate, comprising:

a bus disposed on the first substrate;

a first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and to the bus; and

an isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

24. The device as recited in claim 23, comprising an expansion port disposed on the first substrate and coupled to the bus, wherein the expansion port is connectable to a second substrate, and wherein the second bus controller is disposed on the second substrate.

25. The device as recited in claim 23, wherein the second bus controller is disposed on a second substrate, and the device comprises a cable having a first end and a second end, the first end being connectable to the first substrate, and the second end being connectable to the second substrate.

26. The device as recited in claim 24, comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus.

27. The device as recited in claim 23, comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the first bus controller in response to detection of the second bus controller.

28. The device as recited in claim 23, wherein the isolation device comprises an electronic switch.

29. The device as recited in claim 28, wherein the electronic switch comprises a transistor.

30. The device as recited in claim 23, wherein the processor and the memory are disposed on the first substrate.

31. The device as recited in claim 23, wherein the bus comprises a SCSI bus.

32. The device as recited in claim 31, comprising a SCSI device connectable to the SCSI bus.

33. The device as recited in claim 32, wherein the SCSI device comprises a hard disk drive.

34. The device as recited in claim 23, wherein the device comprises a low profile server.

35. A printed circuit board for a low profile server, the system board comprising:

a substrate;

a bus disposed on the substrate;

a first bus controller disposed on the substrate, the first bus controller coupled to the bus and configured to control the bus; and

an isolation device disposed on the substrate and configured to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

36. The board as recited in claim 35, comprising a termination device disposed on the substrate and configured to terminate the first bus controller in response to detection of the second bus controller coupled to the bus.

37. The board as recited in claim 35, comprising an expansion port disposed on the substrate and coupled to the bus, wherein the second bus controller is coupled to the bus via the expansion port.

38. The board as recited in claim 37, comprising a termination device disposed on the substrate and configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus via the expansion port.

39. The board as recited in claim 35, wherein the isolation device comprises an electronic switch.

40. The board as recited in claim 39, wherein the electronic switch comprises a transistor.

41. The printed circuit board as recited in claim 35, comprising:

a memory disposed on the substrate; and

a processor disposed on the substrate, the processor being coupled to the memory and to the first bus controller.

42. The printed circuit board as recited in claim 35, wherein a SCSI device is coupled to the bus, the SCSI device being controllable by the first bus controller or the second bus controller.

43. The printed circuit board as recited in claim 42, wherein the SCSI device comprises a hard disk drive.

44. A method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:

providing a bus disposed on a substrate;

connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller;

disposing an isolation device on the substrate, the isolation device being connected to the bus; and

disposing a first bus controller on the substrate, the first bus controller being connected to the isolation device, the isolation device being configured to

isolate the first bus controller from the bus when a second bus controller is connected to the expansion port.

45. The method as recited in claim 44, comprising the act of:

disposing a termination device on the substrate, the termination device being connected to the bus.

46. The method as recited in claim 45, wherein the termination device is connected to the bus proximate the first bus controller.

47. The method as recited in claim 46, wherein the termination device is configured to terminate the first bus controller when the second bus controller is connected to the expansion port.

48. The method as recited in claim 45, wherein the termination device is connected to the bus proximate the expansion port.

49. The method as recited in claim 48, wherein the termination device is configured to terminate the bus proximate the expansion port when the second bus controller is not connected to the expansion port.

50. The method as recited in claim 44, wherein the bus comprises a SCSI bus.

51. The method as recited in claim 44, wherein the first bus controller comprises a SCSI bus controller.

52. (previously presented) A method of manufacturing an expansion card connectable to a system controller board having a system bus controller configured to control the bus, and having an isolation device, the method comprising the acts of:

disposing an expansion bus controller on a substrate, the expansion bus controller being configured to control a bus;

disposing a detect signal generator on the substrate;

connecting the detect signal generator to the first expansion connector; and

disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator,

wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board, ~~and~~

wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable, and

wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal.

53. A method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:

electrically coupling a first device to the communications medium;

generating a detection signal indicative of coupling of a second device to the communications medium; and

automatically isolating the first device from the communications medium in response to the detection signal.

54. The method as recited in claim 53, wherein the communications medium comprises a point-to-point interconnect.

55. The method as recited in claim 53, wherein the communications medium comprises shared bus.